IN THE CLAIMS

What is claimed is:

1. A method for making a semiconductor device comprising:

forming a first dielectric layer on a substrate;

forming a trench within the first dielectric layer;

forming a second dielectric layer on the substrate, the second dielectric layer having a first part that is formed at the bottom of the trench and a second part;

forming a first metal layer on the first part of the second dielectric layer, the first metal layer covering the first part of the second dielectric layer but not covering the second part of the second dielectric layer; and

forming a second metal layer on the first metal layer and on the second part of the second dielectric layer, the second metal layer covering the first metal layer and covering the second part of the second dielectric layer.

2. The method of claim 1 wherein the second dielectric layer comprises a high-k gate dielectric layer.

3. The method of claim 2 wherein the high-k gate dielectric layer comprises a material that is selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

4. The method of claim 1 wherein the first metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and the second metal layer comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide.

5. The method of claim 1 wherein the first metal layer comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide and the second metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide.

6. The method of claim 1 wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV, and the second metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV.

7. The method of claim 1 wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV, and the second metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV.

8. The method of claim 1 further comprising forming a fill metal within the trench and on the second metal layer.

9. The method of claim 1 further comprising forming an underlayer metal on the second dielectric layer prior to forming the first metal layer.

10. The method of claim 1 further comprising forming the first metal layer on the first part of the second dielectric layer by forming a metal layer on both the first and second parts of the second dielectric layer, then removing the metal layer from the second part of the dielectric layer.

11. The method of claim 10 wherein the first metal layer is formed on the first part of the second dielectric layer by:

forming a metal layer on both the first and second parts of the second dielectric layer;

forming a spin on glass layer on the metal layer, a first part of the spin on glass layer covering the first part of the second dielectric layer and a second part of the spin on glass layer covering a second part of the second dielectric layer;

removing the second part of the spin on glass layer while retaining the first part of the spin on glass layer, exposing part of the metal layer;

removing the exposed part of the metal layer to generate the first metal layer that covers the first part of the second dielectric layer but does not cover the second part of the second dielectric layer; then

removing the first part of the spin on glass layer.

12. A method for making a semiconductor device comprising:

forming a first dielectric layer on a substrate;

forming a trench within the first dielectric layer;

forming a high-k gate dielectric layer on the substrate, the high-k gate dielectric layer having a first part that is formed at the bottom of the trench and a second part;

forming a metal layer on both the first and second parts of the high-k gate dielectric layer;

forming a spin on glass layer on the metal layer, a first part of the spin on glass layer covering the first part of the high-k gate dielectric layer and a second part of the spin on glass layer covering a second part of the high-k gate dielectric layer;

removing the second part of the spin on glass layer while retaining the first part of the spin on glass layer, exposing part of the metal layer;

removing the exposed part of the metal layer to generate a first metal layer that covers the first part of the high-k gate dielectric layer but does not cover the second part of the high-k gate dielectric layer;

removing the first part of the spin on glass layer; and

forming a second metal layer on the first metal layer and on the second part of the high-k gate dielectric layer, the second metal layer covering the first metal layer and covering the second part of the high-k gate dielectric layer.

13. The method of claim 12 wherein the high-k gate dielectric layer comprises a material that is selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

14. The method of claim 12 wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has

a workfunction that is between about 3.9 eV and about 4.2 eV and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and the second metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV and comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide, and further comprising forming a fill metal within the trench and on the second metal layer.

15. The method of claim 12 wherein the first and second metal layers are each between about 25 and about 300 angstroms thick, the first metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV and comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide and the second metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and further comprising forming a fill metal within the trench and on the second metal layer.

16. A method for making a semiconductor device comprising:

forming a first dielectric layer on a substrate;

forming a trench within the first dielectric layer;

forming a high-k gate dielectric layer on the substrate, the high-k gate dielectric layer having a first part that is formed at the bottom of the trench and a second part, the high-k gate dielectric layer comprising a material that is selected

from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide;

forming a metal layer on both the first and second parts of the high-k gate dielectric layer, the metal layer being between about 25 and about 300 angstroms thick;

forming a spin on glass layer on the metal layer, a first part of the spin on glass layer covering the first part of the high-k gate dielectric layer and a second part of the spin on glass layer covering a second part of the high-k gate dielectric layer;

removing the second part of the spin on glass layer while retaining the first part of the spin on glass layer, exposing part of the metal layer;

removing the exposed part of the metal layer to generate a first metal layer that covers the first part of the high-k gate dielectric layer but does not cover the second part of the high-k gate dielectric layer;

removing the first part of the spin on glass layer; and

forming a second metal layer on the first metal layer and on the second part of the high-k gate dielectric layer, the second metal layer being between about 25 and about 300 angstroms thick and covering the first metal layer and the second part of the high-k gate dielectric layer.

17. The method of claim 16 wherein the first metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and the second metal layer has a workfunction

that is between about 4.9 eV and about 5.2 eV and comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide.

18. The method of claim 16 wherein the first metal layer has a workfunction that is between about 4.9 eV and about 5.2 eV and comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide and the second metal layer has a workfunction that is between about 3.9 eV and about 4.2 eV and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide.

19. The method of claim 16 further comprising forming a fill metal within the trench and on the second metal layer.

20. The method of claim 19 wherein the fill metal comprises a material that is selected from the group consisting of tungsten, aluminum, titanium, and titanium nitride.